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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,055	08/16/2001	Simon Dodd	10007744-1	5019

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EXAMINER	
UMEZ ERONINI, LYNETTE T	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 04/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,055	DODD, SIMON	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-14 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3* is/are allowed.

6)☒ Claim(s) *1,2,4,6-10, and 21-26* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/3/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-14 in Amendment filed 1/5/2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

2. The amendment filed 1/5/2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: In claim 23, "depositing a passivation material on a portion the substrate, wherein the portion of the substrate includes a second portion that free of passivation material." It is unclear how a portion of a substrate includes a passivation materials and the portion of a substrate includes a second portion that is free of passivation material.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 23-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In base claim 23, "depositing a passivation material on a portion the substrate, wherein the portion of the substrate includes a second portion that free of passivation material" lacks support.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 23-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In base claim 23, lines 3-5, "depositing a passivation material on a portion the substrate, wherein the portion of the substrate includes a second portion that free of passivation material" is indefinite because it is unclear how a surface portion includes a passivation material and includes a second portion that is free of passivation material.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawamura et al (US 6,543,884 B1).

Kawamura shows show a plurality of thin films (column 4, lines 19-21), FIGS. **4**, **8**, and **10**A – **10**E, and **11**, which comprises: FOX **92**, PSG **92**, TaAl **62**, Si_3N_4 **96,** SiC **98**, Ta **100**, and Au **114**. Kawamura teaches " . . . Thin film layers, including ink ejection elements (same as applicant's drop generator), are formed on a top surface of a silicon substrate. The various layers are etched to provide conductive leads to the ink ejection elements. At least one ink feed hole is formed through the thin film layers for each ink ejection chamber. A trench is etched in the bottom surface of the substrate so that ink can flow into the trench and into each ink ejection chamber through the ink feed holes formed in the thin film layers. An orifice layer is formed on the top surface of the thin film layers to define the nozzles and ink ejection chambers. A phosphosilicate glass (PSG) layer, providing an insulation layer beneath the resistive layers, is etched back from the ink feed holes and is protected by a passivation layer to prevent the ink from interacting with the PSG layer (Abstract). The aforementioned reads on,

A method of fabricating multiple layer of a thermal injet printhead that includes a substrate and a trench for moving ink across the substrate, as well as drop generator components for ejecting drops of ink form the substrate, comprising the steps of:

masking a first portion of the substrate surface with passivation material having edges that define boundaries on the surface that within the boundaries a second portion is exposed for etching;

depositing a metal layer over the passivation material; and

then etching the second surface portion, **in claim 1**;

wherein the masking step includes depositing a layer of silicon nitride on the substrate surface and then depositing on the silicon nitride a layer of silicon carbide, **in claim 2**;

including the step of underlying the passivation material with a layer of phosphosilicate glass at locations near the boundaries, **in claim 4.**

wherein the masking step includes depositing the passivation material on the substrate surface, **in claim 21**; and

etching the second portion while the passivation material is on the substrate surface, in **claim 22**.

9. Claims 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hawkins (US 4,863,560).

Referring to FIGS. 3-5,

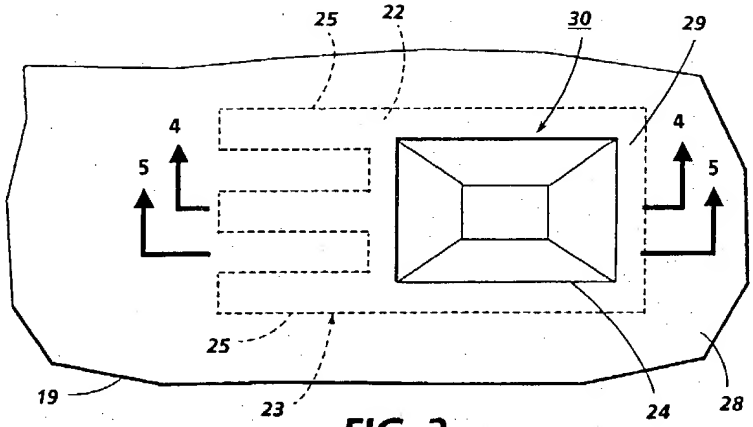

FIG. 3

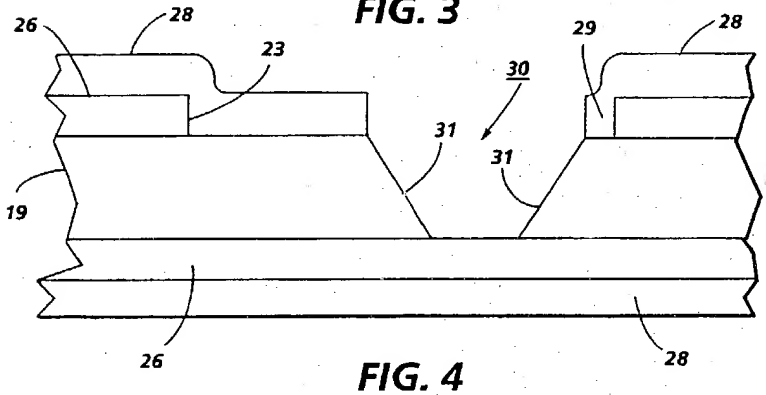

FIG. 4

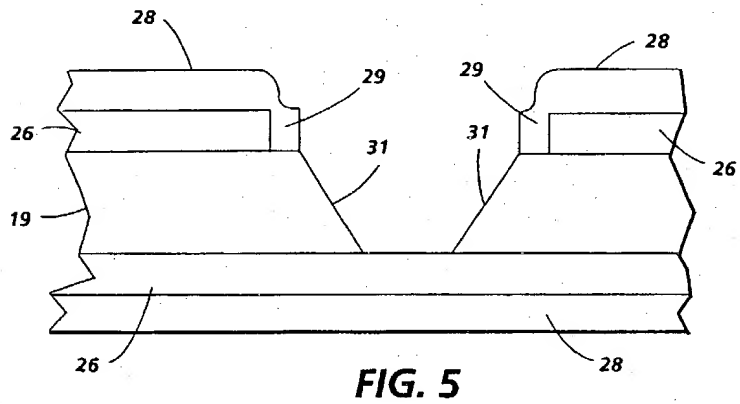

FIG. 5

Hawkins teaches a SiO_2 **26** layer is lithographically processed to form a via **23** on a silicon wafer **19**; a Si_3N_4 layer **28** is deposited over the patterned SiO_2 **26** layer and the exposed silicon wafer surface **22** and the Si_3N_4 layer **28** is then lithographically processed to produce via **24**, so that via **24** exposes the bare silicon surface **22** of wafer **19**. Hawkins further teaches, "Note that a border **29** of Si_3N_4 (see FIG. 5) is left about 1 mil wide inside of the SiO_2 via **23** both for protection and limitation of undercutting during subsequent ODE processing. When the wafer is anisotropically etched, the silicon is etched through where exposed by via **24** to form reservoir recesses **30**" (column 5, lines 43-66 and FIGS. **3-5**). The above reads on,

A method of masking and etching a surface of a silicon substrate, comprising the steps of:

providing on the substrate surface an oxide layer in a pattern having edges that define boundaries of the surface portion such that within the boundaries the surface portion is exposed for etching;

covering the oxide layer near the edges with passivation material; and

etching the surface portion of the silicon substrate that is exposed for etching, **in claim 6**; and

including the step of covering the edges of the oxide layer with passivation material, **in claim 8**.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hawkins (US '560) as applied to claim 6.

Hawkins differs in failing to teach patterning some of the oxide layer to define a part of a transistor gate carried by the substrate, **in claim 7.**

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use a conventional method of forming a gate electrode by growing or depositing an oxide layer on a semiconductor in fabricating a transistor, which comprises a source region, drain region, and gate electrode.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hawkins (US '192) as applied to claim 6 above, and further in view of Kawamura et al. (US 6,543,884 B1).

Hawkins differs in failing to teach temporarily covering the surface portion of the substrate with a layer of phosphosilicate glass that is removed before etching of the surface portion.

Kawamura teaches, a PSG is deposited over a substrate (column 4, lines 26-28) and the PSG is etched to pull back the PSG layer from the ink feed hole so as not to be

in contact with any ink because the PSG layer is vulnerable to certain inks and the etchant used to form a trench (column 4, lines 61-65).

It would have been obvious to modify Hawkins by employing Kawamura's method of covering the surface portion of the substrate with a layer of phosphosilicate glass that is removed before etching of the surface portion for the purpose of protecting the layer from being vulnerable to certain inks and the etchant used to form a trench (Kawamura, column 4, lines 61-65).

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hawkins (US '560) as applied to claim 6 above, and further in view of Hess (US 4,719,477).

Hawkins differs in failing to teach covering the oxide layer with a passivation material includes covering the heat transducer with passivation material.

Hess teaches a method of forming a structure in which a transistor (device that comprises a source, drain, and gate oxide) in one area a silicon substrate and a thermal ink jet printhead resistor (same as applicant's heat transducer) in another area of the substrate and building a resistor, conductor and passivation layers after the resistor logic and drive transistors have been fabricated (column 5, lines 1-12), which reads on wherein the substrate carries a heat transducer and wherein the step of covering the oxide layer with passivation material include covering the heat transducer with passivation material. Hess further teaches, "It is also known in this art to deposit an inert refractory material such as silicon carbide or silicon nitride over the aluminum trace material and the exposed resistive material in order to provide a barrier layer between

the resistive and conductive materials and the ink. This ink is stored in individual reservoirs and heated by thermal energy passing from the individually defined resistors and through the barrier layer to the ink reservoirs atop the barrier layer. The ink is highly corrosive, so it is important that the barrier layer be chemically inert and highly impervious to the ink" (column 1, lines 32-42).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hawkins by using a substrate that carries a heat transducer and a step of covering the oxide layer with passivation material includes covering the heat transducer with passivation material, as taught by Hess for the purpose of providing a chemically inert-barrier layer that is highly impervious to highly corrosive ink (column 1, lines 40-42).

Claim Rejections - 35 USC § 102

14. Claims 11 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawamura et al. (US 6,543,884 B1).

Kawamura teaches, " . . . Thin film layers, including ink ejection elements (same as applicant's drop generator), are formed on a top surface of a silicon substrate. The various layers are etched to provide conductive leads to the ink ejection elements. At least one ink feed hole is formed through the thin film layers for each ink ejection chamber. A trench is etched in the bottom surface of the substrate so that ink can flow into the trench and into each ink ejection chamber through the ink feed holes formed in the thin film layers. An orifice layer is formed on the top surface of the thin film layers

to define the nozzles and ink ejection chambers. A phosphosilicate glass (PSG) layer, providing an insulation layer beneath the resistive layers, is etched back from the ink feed holes and is protected by a passivation layer to prevent the ink from interacting with the PSG layer (Abstract). FIGS. **4**, **8**, and **10**A – **10**E, and **11** show a plurality of thin films (column 4, lines 19-21), which comprises: FOX **92**, PSG **92**, TaAl **62**, Si_3N_4 **96,** SiC **98**, Ta **100**, and Au **114**. The aforementioned reads on,

A method of fabricating multiple layer of a thermal injet printhead that includes a substrate and a trench for moving ink across the substrate, as well as drop generator components for ejecting drops of ink form the substrate, comprising the steps of:

providing a layer on the substrate to serve as a drop generator component; and then etching the substrate to form the trench in the substrate.

Since Kawamura teaches the using the same materials in forming layers on a substrate as the claimed invention, then using Kawamura method of forming a layer on a substrate in the same manner as the claimed invention would result in a layer on the substrate to serve as a mask to define the trench for etching.

Claim Rejections - 35 USC § 103

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura (US '884 B1) as applied to claim 11.

Kawamura differs in failing to teach growing a layer of oxide to serve as a transistor gate component of the drop generator as well as the mask.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use a conventional method of forming a gate electrode by growing or depositing an oxide layer on a semiconductor in fabricating a transistor, which comprises a source region, drain region, and gate electrode and using a conventional photolithographic method in growing a silicon oxide layer to form a hard mask.

16. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura (US '884 B1) as applied to claim 11 above, and further in view of Hawkins (US '560).

Kawamura differs in failing to teach capping the oxide layer near the trench with a layer of passivation material.

Hawkins teaches a SiO_2 **26** layer is lithographically processed to form a via **23** on a silicon wafer **19**; a Si_3N_4 layer **28** is deposited over the patterned SiO_2 **26** layer and the exposed silicon wafer surface **22** and the Si_3N_4 layer **28** is then lithographically processed to produce via **24**, so that via **24** exposes the bare silicon surface **22** of wafer 19. Hawkins further teaches, "Note that a border **29** of Si_3N_4 (see FIG. 5) is left about 1 mil wide inside of the SiO_2 via **23** both for protection and limitation of undercutting during subsequent ODE (orientation etching) processing (column 5, lines 43-64), which reads on, capping the oxide layer near the trench with a layer of passivation material.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Kawamura by using Hawkins method of capping an

oxide layer near the trench for the purpose of protection and limitation of undercutting during subsequent ODE processing (column 5, lines 61-64).

Allowable Subject Matter

17. Claim 3 is allowed.

18. The following is a statement of reasons for the indication of allowable subject matter: No prior art teaches and suggests it would be obvious in masking with the passivation material includes the simultaneous deposition of the passivation material at a location away from the exposed surface portion to enable use of some of the passivation material as one of the drop generator layers as well as the mask, in the sequence of steps in a method of etching a substrate surface, along with the other limitations of claim 3.

19. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is a statement of reasons for the indication of allowable subject matter: No prior art teaches and suggests it would be obvious in fabricating on the substrate drop generator layers that provide for controlled expulsion of liquid from the substrate, wherein the step of covering the passivation material with the metal layer includes the simultaneous deposition of the metal layer at a location away from the exposed surface portion to enable use of some of that metal layer as one of the drop generator layer, in a sequence of steps in a method of etching a substrate surface.

Response to Arguments

21. Applicant's arguments with respect to claims 1, 2, 4-14, and 23-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ltue

March 24, 2004

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER